

A NEW PV BASED CLOSED LOOP CONTROL OF HIGH STEP UP DC-DC CONVERTER

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ABSTRACT

In this paper high boost isolated dc-dc converter with closed loop control to provide high voltage regulation control suitable for renewable energy source is proposed. PV system is used as the renewable source for dc-dc converter. The circuit consists of active clamp circuit and boost converter with coupled inductor. To achieve high output voltage gain the converter output terminal and boost converter output terminal are connected in serially with the isolated inductors with less voltage stress on controlled power switch and power diodes. The operating principles and the steady-state analyses of the proposed converter are discussed in detail. The simulation results are obtained using MATLAB/SIMULINK software.

KEYWORDS: Renewable Energy, High Boost, Active Clamp Circuit

INTRODUCTION

High boost DC-DC converters operating at high voltage regulation are widely proposed in many industrial applications. High boost dc-dc converters [1-4] are play a important role in renewable energy sources such as fuel energy systems, DC-back up energy system for UPS, High intensity discharge lamp and automobile applications. The converters require increasing low dc voltage to high dc voltage. The conventional boost converters are able to get high voltage duty ratio the problem is Electro Magnetic Interference and complexity increases. In this proposed method high boost topology proposed [4] with closed loop control. Output voltage controlled with better voltage regulation for various changes in the load conditions.

DC-DC converters [1] with coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors [2]. The solution would be the use of transformers to get the preferred voltage conversion ratio similar in forward or fly back converter the dc-isolation is no need for industrial applications. To suppress the high voltage spike on power switch non dissipative snubber and active clamp circuit is used. The active clamp circuit clamps the surge voltage of switches and recycles the energy stored in the leakage inductance of the transformer [5]. The leakage energy of the coupling inductor recycles the energy. Without wasting through active clamp, active clamp circuit consists a clamped diode and clamped capacitor. The clamped-voltage dc-dc converter [1] with reduced reverse recovery current and switch-voltage stress. The active switch in the converter can still sustain a proper duty ratio when even under high step-up [2-3] applications, reducing voltage and current stresses voltage gain with high significantly. The concept of two capacitors charged voltage duty ratio then problem is Electro Magnetic parallel and discharged in series via the coupled inductor to achieve high boost [5-7] voltage stress on the main switch can be reduced, analysis and implementation done in the boost converter [4-7] output terminal and flyback converter output terminal are serially connected to increase the output voltage gain with the coupled inductor.

OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Figure 1 shows the circuit configuration of the proposed converter, which consists of two active switches S_1 and

S_2 , one coupled inductor, four diodes D_1 – D_4 , and two output capacitors C_1 and C_2 .

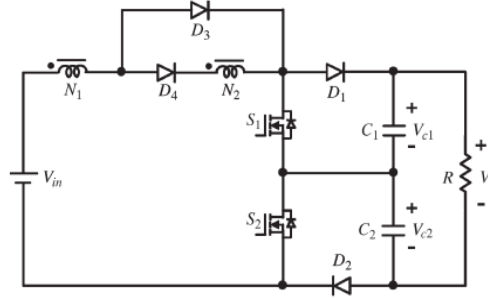


Figure 1: Circuit Configuration of the Proposed Converter

The simplified circuit model of the proposed converter is shown in Figure 2. The coupled inductor is modeled as a magnetizing inductor L_m , a primary leakage inductor L_{k1} , a secondary leakage inductor L_{k2} , and an ideal transformer. Capacitors C_{S1} and C_{S2} are the parasitic capacitors of S_1 and S_2 , respectively.

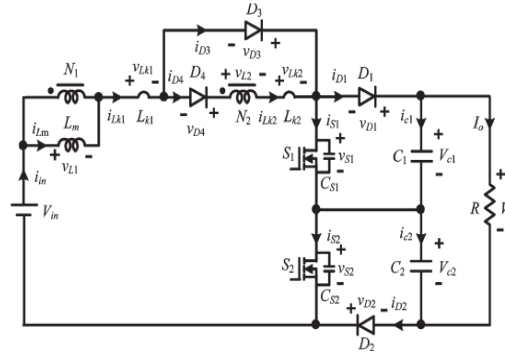


Figure 2: Simplified Circuit Model of the Proposed Converter

In order to simplify the circuit analysis of the proposed converter, some conditions are assumed as follows. First, all components are ideal. The ON-state resistance $R_{DS(ON)}$ of the active switches, the forward voltage drop of the diodes, and the ESR of the coupled inductor and output capacitors are ignored. Second, output capacitors C_1 and C_2 are sufficiently large, and the voltages across C_1 and C_2 are considered to be constant during one switching period. Figure 3 shows some typical waveforms during one switching period in continuous-conduction-mode (CCM) operation.

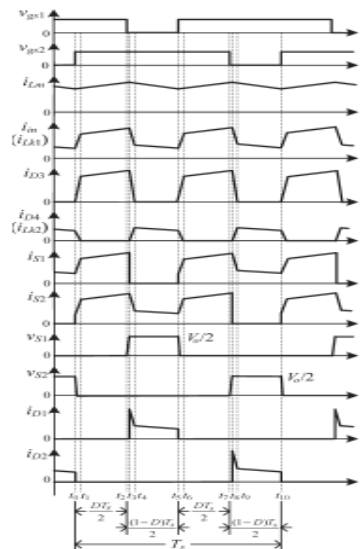


Figure 3: Some Typical Waveforms of the Proposed Converter at CCM Operation

The operating principle is described as follows.

Mode I [t_0, t_1]: At $t = t_0$, S_1 and S_2 are turned on. The current-flow path is shown in Figure 4(a). The dc-source energy is transferred to L_m and L_{k1} through D_3 , S_1 , and S_2 , so currents i_{Lm} , i_{Lk1} , and i_{D3} are increased. The energy stored in L_{k2} is released to L_m and L_{k1} through D_4 , S_1 , and S_2 . Thus, i_{Lk2} is decreased. Meanwhile, the energy stored in L_{k2} is recycled. The energy stored in C_{S2} is rapidly and completely discharged. The energies stored in C_1 and C_2 are discharged to the load. This mode ends when i_{Lk2} is equal to zero at $t = t_1$.

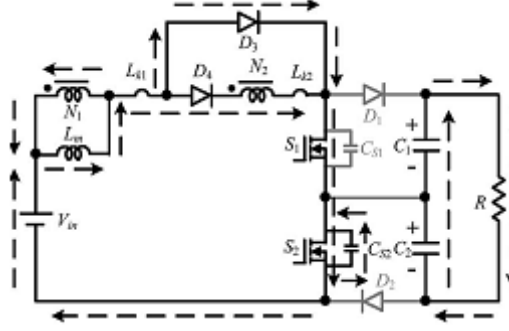


Figure 4(a)

Mode II [t_1, t_2]: In this mode, S_1 and S_2 are still turned on. The current-flow path is shown in Figure 4(b). The dc source energy is still transferred to L_m and L_{k1} . Thus, i_{Lm} and i_{Lk1} are still increased. The energies stored in C_1 and C_2 are still discharged to the load.

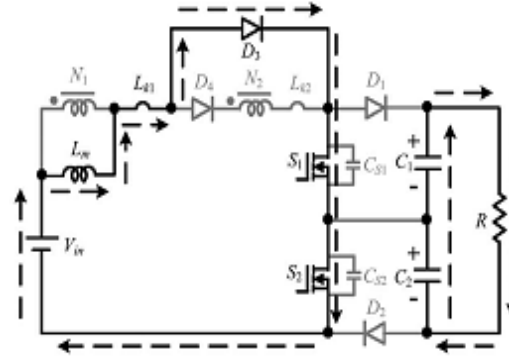


Figure 4(b)

Mode III [t_2, t_3]: At $t = t_2$, S_1 is turned off, and S_2 is still turned on. The current-flow path is shown in Figure 4(c). The dc-source energy is still transferred to L_m , L_{k1} , and C_{S1} . Meanwhile, the voltage across S_1 is increased rapidly. The energies stored in C_1 and C_2 are still discharged to the load.

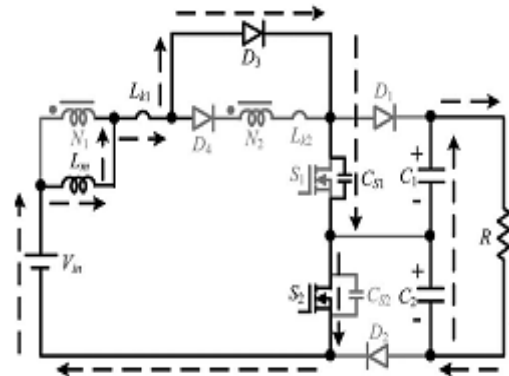


Figure 4(c)

Mode IV [t_3, t_4]: During this time interval, S_1 is still turned off, and S_2 is still turned on. The current-flow path is shown in Figure 4(d). The dc source, L_m , and L_{k1} are series connected to transfer their energies to L_{k2} , C_1 , and the load. Thus, i_{Lm} and i_{Lk1} are decreased, and i_{Lk2} is increased. Meanwhile, the energy stored in L_{k1} is recycled to C_1 and the load. The energy stored in C_2 is still discharged to the load. This mode ends when i_{Lk1} is equal to i_{Lk2} at $t = t_4$.

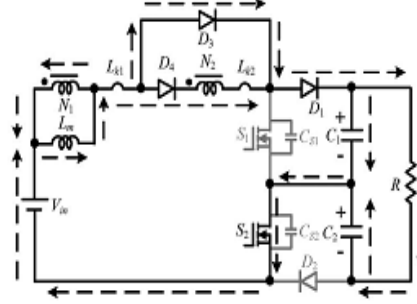


Figure 4(d)

Mode V [t_4, t_5]: During this period, S_1 is still turned off, and S_2 is still turned on. The current-flow path is shown in Figure 4(e). The dc source, L_m , L_{k1} , and L_{k2} are series connected to transfer their energies to C_1 and the load. Thus, i_{Lm} , i_{Lk1} , and i_{Lk2} are decreased. The energy stored in C_2 is still discharged to the load.

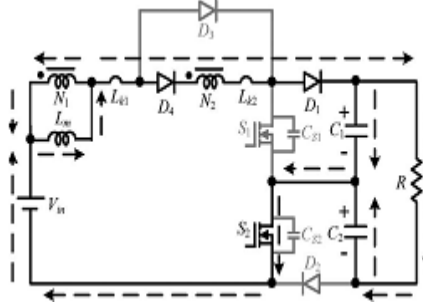


Figure 4(e)

Mode VI [t_5, t_6]: At $t = t_5$, S_1 and S_2 are turned on. The current-flow path is shown in Figure 4(f). The dc-source energy is transferred to L_m and L_{k1} through D_3 , S_1 , and S_2 . Therefore, currents i_{Lm} , i_{Lk1} , and i_{D3} are increased. The energy stored in L_{k2} is released to L_m and L_{k1} through D_4 , S_1 , and S_2 . Thus, i_{Lk2} is decreased. Meanwhile, the energy stored in L_{k2} is recycled. The energy stored in C_{S1} is rapidly and completely discharged. The energies stored in C_1 and C_2 are discharged to the load. This mode ends when i_{Lk2} is equal to zero at $t = t_6$.

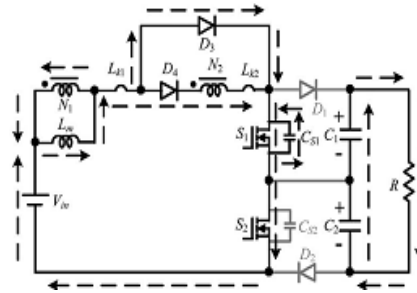


Figure 4(f)

Mode VII [t_6, t_7]: During this time interval, S_1 and S_2 are still turned on. The current-flow path is shown in Figure 4(g). The dc-source energy is still transferred to L_m and L_{k1} . Thus, i_{Lm} and i_{Lk1} are still increased. The energies stored in C_1 and C_2 are still discharged to the load.

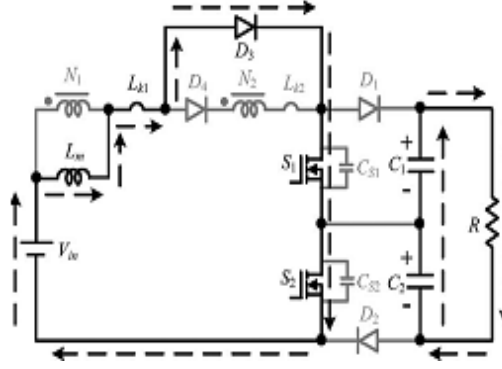


Figure 4(g)

Mode VIII [$t7, t8$]: At $t = t7$, S_1 is still turned on, and S_2 is turned off. The current-flow path is shown in Figure 4(h). The dc-source energy is still transferred to L_m , L_{k1} , and C_{S2} . Meanwhile, the voltage across S_2 is increased rapidly. The energies stored in C_1 and C_2 are still discharged to the load.

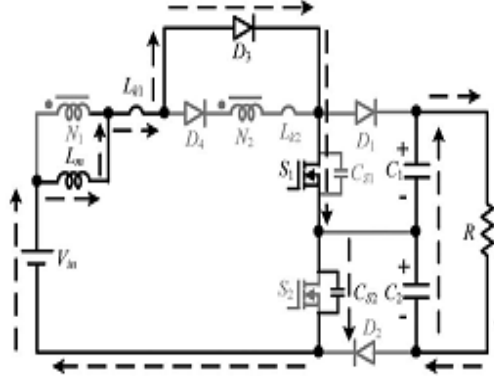


Figure 4(h)

Mode IX [$t8, t9$]: During this period, S_1 is still turned on, and S_2 is still turned off. The current-flow path is shown in Figure 4(i). The dc source, L_m , and L_{k1} are series connected to transfer their energies to L_{k2} , C_2 , and the load. Thus, i_{Lm} and i_{Lk1} are decreased, and i_{Lk2} is increased. Meanwhile, the energy stored in L_{k1} is recycled to C_2 and the load. The energy stored in C_1 is still discharged to the load. This mode ends when i_{Lk1} is equal to i_{Lk2} at $t = t9$.

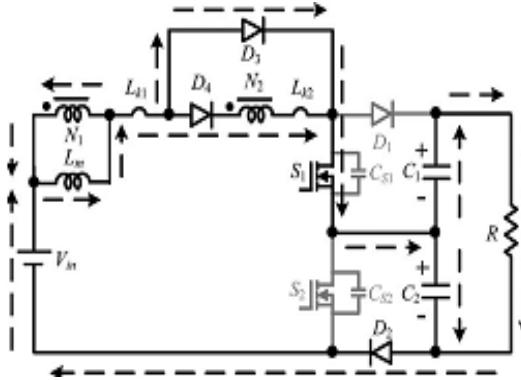


Figure 4(i)

Mode X [$t9, t10$]: In this mode, S_1 is still turned on, and S_2 is still turned off. The current-flow path is shown in Figure 4(j). The dc source, L_m , L_{k1} , and L_{k2} are series connected to transfer their energies to C_2 and the load. Thus, i_{Lm} , i_{Lk1} , and i_{Lk2} are decreased. The energy stored in C_1 is still discharged to the load. This mode ends when S_1 and S_2 are turned on at the beginning of the next switching period.

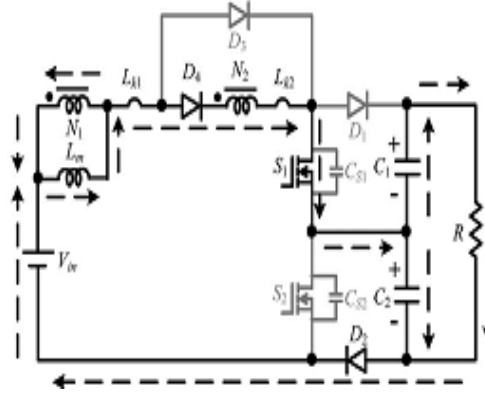


Figure 4(j)

STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

Voltage Gain

At CCM operation, the time durations of modes I, III, IV,

VI, VIII, and IX are very short as compared to one switching period. Thus, only modes II, V, VII, and X are considered. At modes II and VII, the following equations can be written from Figure 4(b) and (g):

$$v_{L1}^{II} = v_{L1}^{VII} = kV_{in} \quad (1)$$

$$\frac{di_{Lm}^{II}}{dt} = \frac{di_{Lm}^{VII}}{dt} = \frac{kV_{in}}{L_m} \quad (2)$$

Where the coupling coefficient k of the coupled inductor is equal to $L_m/(L_m + L_{k1})$. At mode V, the following equations are derived from Figure 4(e):

$$i_{Lk1}^V = i_{Lk2}^V \quad (3)$$

$$i_{Lm}^V = (1 + n)i_{Lk1}^V \quad (4)$$

$$V_{in} - V_{c1} = v_{L1}^V + v_{Lk1}^V + v_{L2}^V + v_{Lk2}^V \quad (5)$$

Where the turns ratio n of the coupled inductor is equal to

N_2/N_1 . Voltage v_{Lk2}^V is found to be

$$v_{Lk2}^V = L_{k2} \frac{di_{Lk2}^V}{dt} = L_{k2} \frac{di_{Lk1}^V}{dt} = n^2 L_{k1} \frac{di_{Lk1}^V}{dt} = n^2 v_{Lk1}^V \quad (6)$$

Substituting (6) into (5) yields the following equation:

$$V_{in} - V_{c1} = (1 + n)v_{L1}^V + (1 + n^2)v_{Lk1}^V \quad (7)$$

Voltage v_{L1}^V is written as

$$v_{L1}^V = L_m \frac{di_{Lm}^V}{dt} = (1+n)L_m \frac{di_{Lk1}^V}{dt}. \quad (8)$$

Thus

$$v_{Lk1}^V = L_{k1} \frac{di_{Lk1}^V}{dt} = \frac{L_{k1}}{(1+n)L_m} v_{L1}^V = \frac{1-k}{(1+n)k} v_{L1}^V \quad (9)$$

Substituting (9) into (7) yields the following equation:

$$v_{L1}^V = \frac{(1+n)k}{1+2nk+n^2} (V_{in} - V_{c1}) \quad (10)$$

$$\frac{di_{Lm}^V}{dt} = \frac{(1+n)k}{1+2nk+n^2} \times \frac{V_{in} - V_{c1}}{L_m}. \quad (11)$$

Similarly, at mode X, the voltage across L_m is derived from Figure 4(j) as follows:

$$v_{L1}^X = \frac{(1+n)k}{1+2nk+n^2} (V_{in} - V_{c2}) \quad (12)$$

$$\frac{di_{Lm}^X}{dt} = \frac{(1+n)k}{1+2nk+n^2} \times \frac{V_{in} - V_{c2}}{L_m}. \quad (13)$$

Using the volt-second balance principle on L_m , the following equation is derived:

$$\int_0^{\frac{DT_s}{2}} v_{L1}^{II} dt + \int_0^{\frac{(1-D)T_s}{2}} v_{L1}^V dt + \int_0^{\frac{DT_s}{2}} v_{L1}^{VI} dt + \int_0^{\frac{(1-D)T_s}{2}} v_{L1}^X dt = 0. \quad (14)$$

Substituting (1), (10), and (12) into (14), the voltage gain is obtained as

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2(1+n-nD+n^2D+2nDk)}{(1-D)(1+n)}. \quad (15)$$

Thus, the plot of the voltage gain versus the duty ratio under various coupling coefficients of the coupled inductor is shown in Figure 5.

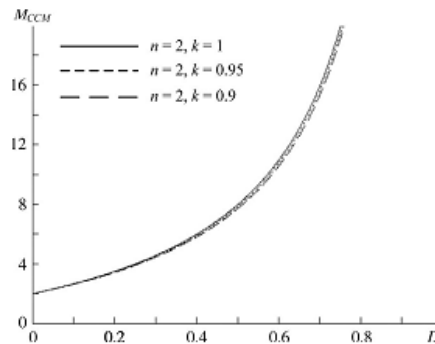


Figure 5: Voltage Gain versus Duty Ratio of the Proposed Converter at CCM Operation with $n=2$ and various Values for k

It can be seen that the voltage gain is not very sensitive to the coupling coefficient. If the impact of the leakage inductor of the coupled inductor is neglected, then coupling coefficient k is equal to one. Substituting $k=1$ into (15), the voltage gain becomes

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2(1+nD)}{1-D}. \quad (16)$$

Boundary Operating Condition

Figure 6 shows some waveforms of the proposed converter at boundary conduction mode (BCM). When the proposed converter is operated in BCM, the peak value of the magnetizing inductor current is given as

$$I_{Lmp} = \frac{kDV_{in}T_s}{2L_m}. \quad (17)$$

Since the time duration $[t_1, t_3]$ is very short as compared to one switching period, this time duration is not considered. The average value of i_{D1} is found to be

$$I_{D1} = \frac{\frac{1}{2} \times \frac{I_{Lmp}}{1+n} \times \frac{1-D}{2} T_s}{T_s} = \frac{(1-D)I_{Lmp}}{4(1+n)}. \quad (18)$$

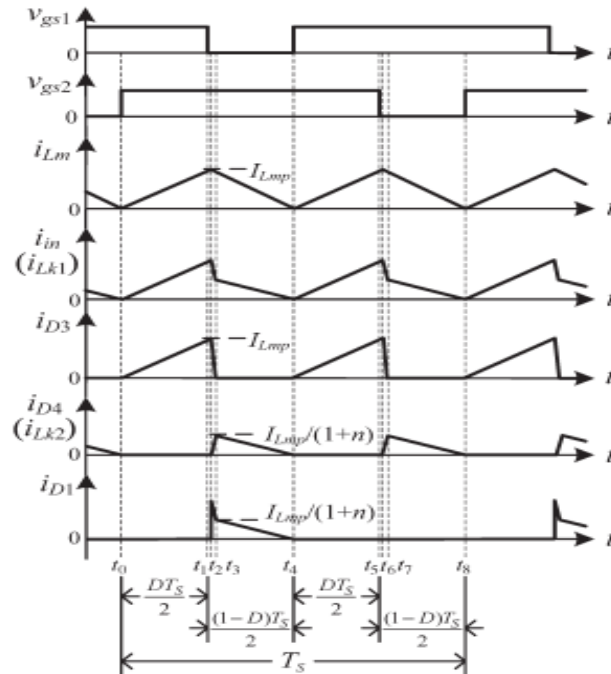


Figure 6: Some Typical Waveforms of the Proposed Converter at BCM Operation

At steady state, the average value of i_{D1} is equal to I_o . Thus

$$\frac{(1-D)I_{Lmp}}{4(1+n)} = I_o = \frac{V_o}{R}. \quad (19)$$

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau_{Lm} \equiv \frac{L_m}{RT_s} = \frac{L_m f_s}{R} \quad (20)$$

Where f_s is the switching frequency.

Substituting (15), (17), and (20) into (19), the boundary normalized magnetizing-inductor time constant LmB can be derived as

$$\tau_{LmB} = \frac{kD(1-D)^2}{16(1+n-nD+n^2D+2nDk)} \quad (21)$$

The curve of τ_{LmB} is shown in Figure 7. If τ_{Lm} is larger than τ_{LmB} , the proposed converter is operated in CCM.

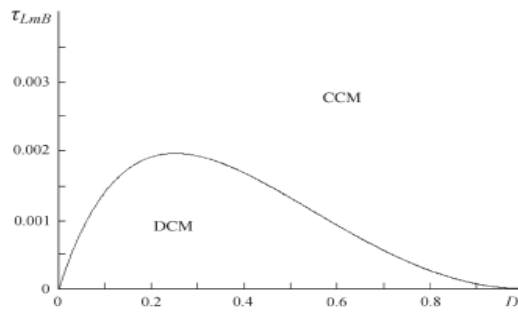


Figure 7: Boundary Condition of the Proposed Converter with $N=2$ and $K=1$

PV CELL MODELLING AND MPPT

A PV cell is the basic structural unit of the PV module that generates current carriers when sunlight falls on it [11]. The power generated by these PV cell is very small. To increase the output power the PV cells are connected in series or parallel to form PV module [12]. The equivalent circuit of the PV cell is shown in Figure 2.

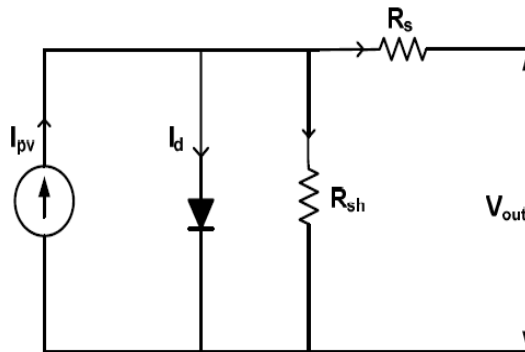


Figure 8: Equivalent Circuit of the PV Cell

The main characteristics of the PV cell are given by:

$$I = I_{pv} - I_o \left[\exp \left(\frac{q(V + IR_s)}{\alpha KT} \right) - 1 \right] - \frac{V + IR_s}{R_{sh}}$$

$$I_o = I_{o,n} \left(\frac{T_n}{T} \right)^3 \exp \left[\frac{qE_g}{\alpha K} \right] \left(\frac{1}{T_n} - \frac{1}{T} \right)$$

$$I_{pv} = [I_{sc} + K_i(T - T_n)] \frac{G}{G_n}$$

Where,

I and V - Cell output current and voltage;

I_0 - Cell reverse saturation current;

T - Cell temperature in Celsius;

K - Boltzmann's constant;

q - Electronic charge;

K_i - short circuit current/temperature coefficient;

G - Solar radiation in W/m^2 ;

G_n - nominal solar radiation in W/m^2 ;

E_g - energy gap of silicon;

$I_{0,n}$ - nominal saturation current;

T_n - nominal temperature in Celsius;

R_s - series resistance;

R_{sh} - shunt resistance;

α - ideality factor between 1.0 to 1.5;

I_{pv} - light generated current;

The I-V characteristic of a PV module shown in Figure.4 is highly non-linear in nature. This characteristics drastically changes with respect to changes in the solar radiation and temperature. Whereas the solar radiation mainly affects the output current, the temperature affects the terminal voltage. The I-V characteristics of the PV module under varying solar radiation at temperature $T=25^0$ is shown below[12].The data of the PV system used in this are taken from **msx60i** type of panels.

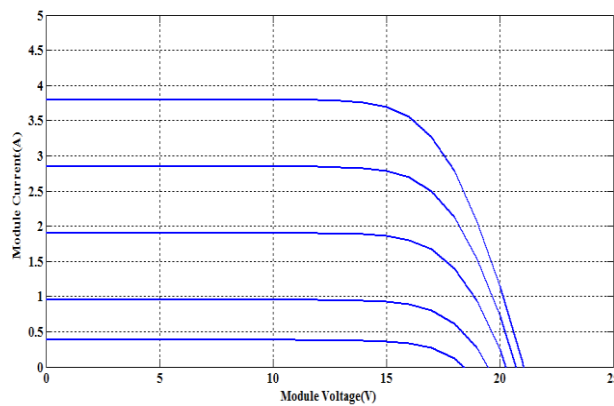


Figure 9: Current Versus Voltage at Constant Cell Temperature $T=25^0$, Irradiation $G=100, 250, 500, 750, 1000 W/m^2$

Figure 5 shows the I-V characteristics of the PV module under varying cell temperature at constant solar radiation ($1000 W/m^2$).

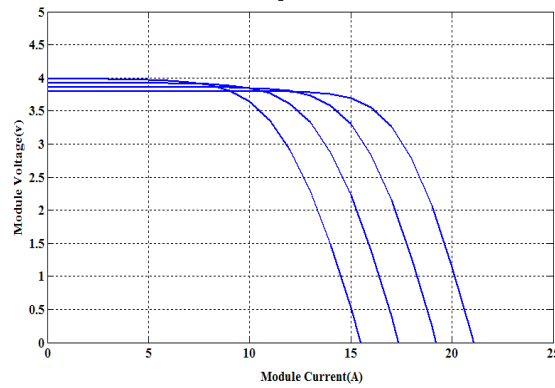


Figure 10: Current versus Voltage at Constant Solar Radiation
 $G = 1000 \text{ W/m}^2, t=25,50,75,100\text{deg Cent}$

MAXIMUM POWER POINT TRACKING (MPPT)

The PV array will be having only one point on its current and voltage characteristics, and that point is called as the Maximum Power Point. The systems which are connected directly will not operate at MPP. So significant amount of energy is wasted because of this problem. But systems which have a DC-DC converter as a controller to match PV array to Pump set will definitely act at MPP. Several MPPT strategies have been proposed in the past like

- Voltage Reference MPPT
- Perturb and Observe(P&O) MPPT
- Incremental Conductance(INC) MPPT

In this paper Perturb and Observe type of MPPT is used for calculating the Duty Cycle for the DC-DC converter. The flowchart of the MPPT algorithm is shown below in Figure 6.

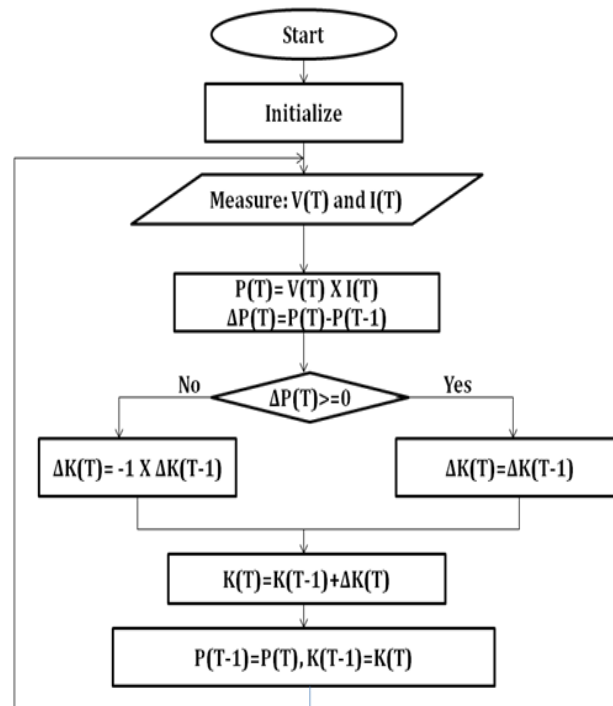


Figure 11: Flow Chart of P&O MPPT Algorithm

The below figure 7 shows the working behavior of P&O based MPPT method.

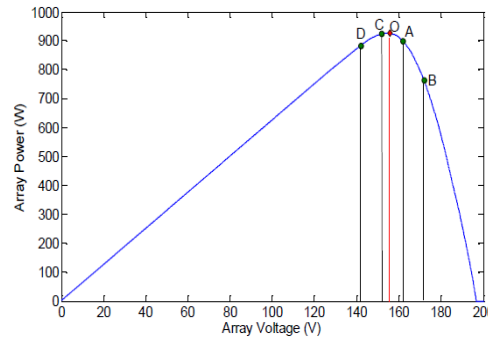


Figure 12: MPPT Tracking

When compared with the other MPPT algorithms P&O algorithm is simpler to implement and it does not need much knowledge of the previous PV array and details about irradiance and temperature. There are two methods of P&O algorithm

- Reference Voltage Perturbation
- Direct Duty ratio Perturbation

The block diagrams of each method are discussed below Figure 8 and Figure 9. In the reference voltage control taking the inputs of voltage and current of the PV system, then implementing to MPPT algorithm, the reference PV voltage is found out. The obtained reference voltage is compared with the actual PV voltage and error is given to PI controller to calculate the duty cycle for DC-DC converter [1].

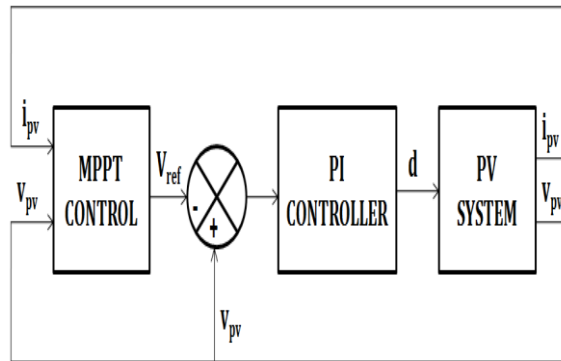


Figure 13: Block Diagram of Reference Voltage Based MPPT

In the Direct Duty Ratio control method the voltage and current inputs from the PV array are taken and the flowchart shown is implemented to calculate the duty cycle for DC-DC converter. When compared with the reference voltage method duty cycle method have several advantages like better stability characteristics and good energy utilization performance.

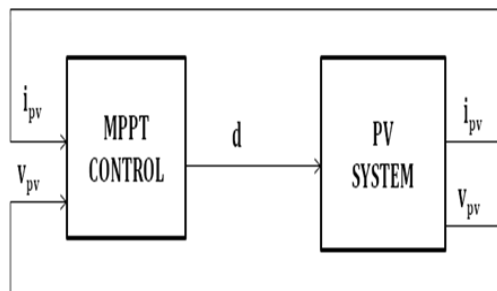


Figure 14: Block Diagram of Direct Duty Ratio Based MPPT

MATLAB/SIMULATION RESULTS

The below figure shows the Matlab/Simulink model of Open loop controlled Converter

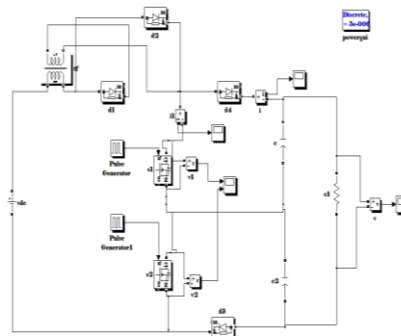


Figure 15: Matlab/Simulink Model of Open Loop Converter

The below figure shows the Gating pulses generated to the switches S1 and S2 to Operate in Open loop

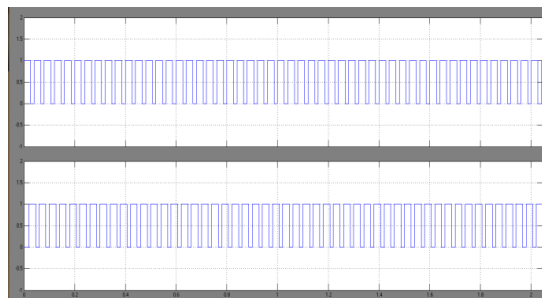


Figure 16: Gating Pulses Generated for Switches S1 and S2

The below figure shows the Voltage across the Switches S1 and S2

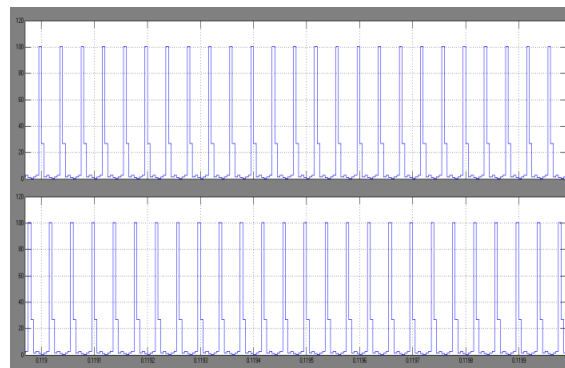


Figure 17: Voltage across Switches S1 and S2

The below figure shows the Voltage across load in the Open loop Operation to Converter

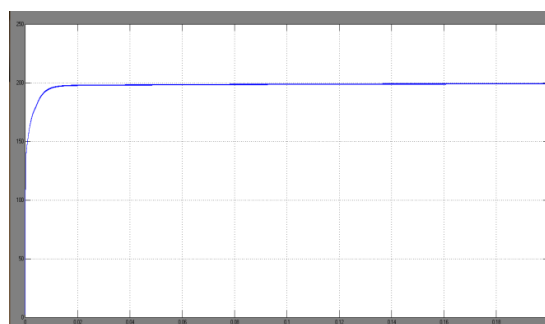


Figure 18: Simulated Output Voltage Wave Form across the Load in Open Loop Operation

The below figure shows the Matlab/Simulink model of Closed loop Operated Converter

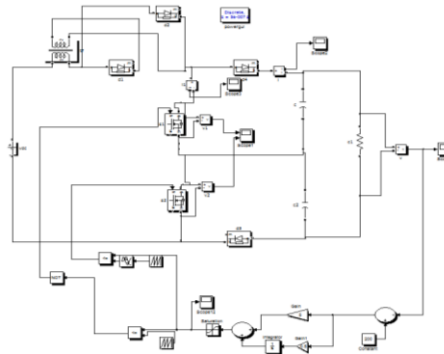


Figure 19: Matlab/Simulink Model of Closed Loop Converter

The below Figure shows the Voltage across the Switches S1 and S2 in Closed loop Operation

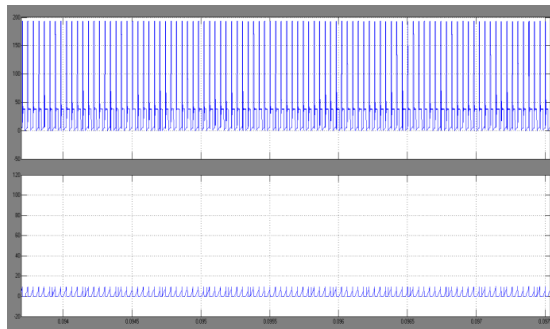


Figure 20: Voltage across the Switches S1 and S2

The below figure shows the Voltage across the load in Closed loop operation

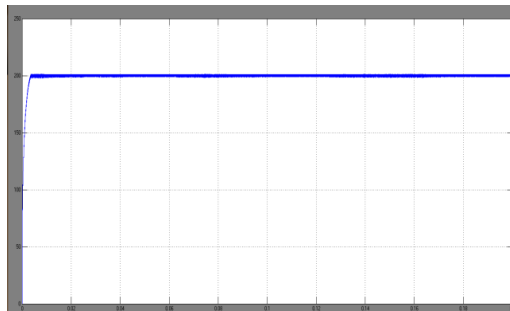


Figure 21: Simulated Output Voltage Wave form across the Load in Closed Loop Operation

CONCLUSIONS

A novel high step-up dc–dc converter has been presented in this paper. The coupled-inductor and voltage-doubler circuits with closed loop operation are integrated in the proposed converter to achieve high step up voltage gain in variable form. The energy stored in the leakage inductor of the coupled inductor can be recycled. The voltages across the switches are half the level of the output voltage during the steady-state period. However, the voltages have the ringing phenomenon at the beginning when the switches are turned off. One must consider this phenomenon for choosing the switches. Similarly, since the ringing phenomenon occurred in the current through diode $D4$, this phenomenon is also considered for choosing diode $D4$. The measured efficiency is 91.1% at the full load condition, and the maximum efficiency is 92.8% at the half-load condition. Comparing the proposed closed loop converter and the conventional converter, one can see that the Variable DC from the converter as per the requirement.

REFERENCES

1. Wai, R.J., L.W. Liu and R.Y. Duan, 2005. 'High- efficiency voltage-clamped DC–DC converter with reduced reverse-recovery current and switch voltage stress', IEEE Trans. Ind. Electron., 53(1): 272-280.
2. Zhao, Q. and F.C. Lee, 2003. 'High-efficiency, high step-up dc-dc converters', IEEE Trans. Power Electron., 18(1): 65-73.
3. Tseng, K.C. and T.J. Liang, 2004. 'Novel highefficiency step-up converter' IEE Proc Inst. Elect. Eng. Electr. Power Appl., 151(2): 182-190.
4. Tseng, K.C. and T.J. Liang, 2005. 'Analysis of intergrated boost-flyback step-up converter', IEE Proc. Inst. Elect. Eng. Electr. Power Appl., Alcazar, E.H.P, 152(2): 217-2222.
5. Kwon, J.M. and B.H. Kwon, 2009. 'High step-upactive-clamp converter with input-current doubler and output-voltage doubler for fuel cell power the systems', IEEE Trans. Power Electron., 24(1): 108-115.
6. Hsieh¹, Y.P., J.F. Chen, T.J. Liang¹ and L.S. Yang, 2012. 'Analysis and implementation of a novel single-switch high step-up DC–DC converter' IET Power Electron., 5(1): 11-21.
7. Wu, T.F., Y.S. Lai, J.C. Hung and Y.M. Chen, 2008. 'Boost converter with coupled inductors and sources. buck–boost type of active clamp', IEEE Trans. Ind. Electron., 55(1): 154-162.

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